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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,244	03/12/2004	Warren M. Farnworth	MI22-2488	8217

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EXAMINER	
CHEN, TSE W	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 11/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,244	FARNWORTH ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 14-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 14-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09012005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated September 1, 2005.

2. Claims 1-7 and 14-38 are presented for examination. Applicant has canceled claims 8-13 and 39-40.

Terminal Disclaimer

3. The terminal disclaimer filed on September 1, 2005 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US Patent 6715018 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on September 1, 2005 was filed before the mailing date of the final Office Action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

5. Claims 3-5 are objected to because of the following informalities: "the computer" should be "the system". Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-5 and 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwa, US Patent 4863232, in view of Swirhun et al., US Patent 5631988, hereinafter Swirhun.

8. In re claim 1, Kwa discloses a system comprising:

- A housing (Figure 1, Item 110).
- A circuit board supported in the housing (Figure 1, Item 114).
- A plurality of slot connectors supported on the circuit board (Figure 1, Item 116).
- A first card in one of the slot connectors (Figure 1, Item 140).
- A first circuit component mounted on the first card (Column 1, Lines 11-22).
- A second card in another one of the slot connectors (Figure 1, Item 140).
- A second circuit component mounted on the second card (Column 1, Lines 11-22).
- An optical interconnect coupling the first card to the second card (Figure 1, Item 130), the first circuit component being configured to communicate with the second circuit component via the optical interconnect (Column 1, Lines 11-22), whereby the optical interconnect does not pass through the slot connectors so that interference that could otherwise be caused by signals to and from the first circuit component is impeded (Column 6, Lines 51-62).

9. Kwa did not disclose the optical interconnect being entirely supported by the first and second cards.

10. Swirhun discloses a system [fig.4a] comprising an optical interconnect [optical fiber ribbon] coupling the first card [400] to the second card [410], the first circuit component [405] being configured to communicate with the second circuit component [415] via the optical

interconnect, the optical interconnect being entirely supported by the first and second cards [col.7, ll.5-28].

11. It would have been obvious to one of ordinary skill in the art, having the teachings of Kwa and Swirhun before him at the time the invention was made, to modify the system taught by Kwa to include the teachings of Swirhun, in order to obtain the claimed optical interconnect. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to alleviate misalignment problems due to thermal strain [Swirhun: col.1, l.63 – col.2, l.16].

12. Regarding Claims 2 and 25, Kwa further discloses optically coupling the first card to the second card comprises using a fiber optic cable (Figure 1, Item 130).

13. Regarding Claims 3-5 and 26-28, Kwa further discloses wherein the optical interconnect comprises a first optical connector, on the first card, configured to convert between electrical signals and optical signals, wherein the system further includes circuit traces on the first card coupling the first optical connector to the first circuit component, wherein the optical interconnect further comprises an optical connector, on the second card, configured to convert between electrical signals and optical signals, the system further including circuit traces on the second card coupling the second optical connector to the second circuit component (Column 1, Lines 11-22; the first and second cards have transmitting and receiving circuitry connected to further circuitry crafted in this matter).

14. In re claim 24, Kwa discloses a method of assembling a system, the method comprising:

- Supporting a circuit board (Figure 1, Item 114) in a housing (Figure 1, Item 110).
- Supporting a plurality of slot connectors on the circuit board (Figure 1, Item l 16).

- Mounting a first circuit component (Column 1, Lines 11-22) on a first card (Figure 1, Item 140).
- Inserting the first card into a first one of the slot connectors (Column 4, Lines 29-30).
- Mounting a second circuit component (Column 1, Lines 11-22) on a second card (Figure 1, Item 140).
- Inserting the second card into a second one of the slot connectors (Column 4, Lines 29-30).
- Flexibly optically coupling the first card to the second card for optical communications between the first circuit component and the second circuit component (Figure 1, Item 130; Column 1, Lines 11-22; the optical coupling is clearly flexible in the figure), whereby the flexible optical interconnect does not pass through the slot connectors so that interference that could otherwise be caused by signals to and from the first circuit component is impeded (Column 6, Lines 51-62).

15. Kwa did not disclose using a first optical connector supported by the first card and completely movable with the first card, a second optical connector supported by the second card and completely movable with the second card, and an optical cable coupled between the first and second optical connectors.

16. Swirhun discloses a method of assembling a system [fig.4a], the method comprising flexibly optically coupling the first card [400] to the second card [410] for optical communications between the first circuit component [e.g., 405, components on 400] and the second circuit component [e.g., 415, components on 410], using a first optical connector [405] supported by the first card and completely movable with the first card [405 attached to 400], a

second optical connector [415] supported by the second card and completely movable with the second card [415 attached to 410], and an optical cable [optical fiber ribbon] coupled between the first and second optical connectors [col.7, ll.5-28].

17. It would have been obvious to one of ordinary skill in the art, having the teachings of Kwa and Swirhun before him at the time the invention was made, to modify the system taught by Kwa to include the teachings of Swirhun, in order to obtain the claimed method. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to alleviate misalignment problems due to thermal strain [Swirhun: col.1, l.63 – col.2, l.16].

18. Claims 6-7 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwa and Swirhun as applied to claims 1 and 24 above, and further in view of Kimmel (4,704,599) and Gillingham (SLDRAM: High-Performance Open-Standard Memory).

19. Regarding Claims 6, 7, 29 and 30, Kwa and Swirhun taught each and every limitation as discussed above in reference to claims 1 and 24. Kwa and Swirhun did not disclose explicitly that the circuit components comprise memory.

20. Kimmel teaches the first or second circuit component comprises a memory (Column 2, Lines 19-22).

21. Kimmel is motivated to allow for the removal of a single card in a system containing a plurality of such cards without affecting the remainder of the system (Column 1, Lines 34-38).

22. Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate the very well known teaching regarding memory in circuit components of Kimmel into the system disclosed by Kwa and Swirhun for the benefit of

allowing single cards in the multiple card system to be removed without affecting the performance of the remainder of the system.

23. Kimmel does not specify the memory device to be a DRAM or a SLDRAM memory device.

24. Gillingham teaches synchronous link DRAM (Pages 29-39 meets the high data bandwidth requirements of emerging processor architectures and retains the low cost of earlier DRAM interface standards (Page 29, Column 1, Paragraph 2).

25. Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of invention to further combine the teachings of SLDRAM as presented by Gillingham into the system so as to make use of memory that can support emerging processor architecture while still maintaining a low degree of cost.

26. Claims 14-16, 18-21, 23, 31-33 and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwa, in view of Kimmel (4,704,599) and Gillingham (SLDRAM: High-Performance Open-Standard Memory).

27. Regarding Claims 14, 19, 31 and 35, Kwa discloses a method and a computer comprising:

- Supporting a circuit board (Figure 1, Item 114) in a housing (Figure 1, Item 110).
- Supporting a plurality of slot connectors (Figure 1, Item 116) on the circuit board (Figure 1, Item 114).
- Supporting a first circuit component (Column l, Lines 11-22) on a first card (Figure 1, Item 140) having an edge connector (Figure 1, Item 142).

- Inserting the edge connector of the first card into a first one of the slot connectors to support the first card from the circuit board (Column 4, Lines 29-30).
- Providing a second card (Figure 1, Item 140) having an edge connector (Figure 1, Item 142) configured for sliding receipt in a second one of the slot connectors (Column 4, Lines 29-30).
- Supporting a second circuit component (Column 1, Lines 11-22) on a second card having an edge connector.
- Inserting the edge connector of the second card into a second one of the slot connectors to support the second card from the circuit board (Column 4, Lines 29-30).
- Optically coupling the first circuit component to the second circuit component for data communications using an optical interconnect within the housing (Figure 1, Item 130; Column 1, Lines 11-22), wherein the optical interconnect does not pass through the slot connectors (Column 1, Lines 51-62).

28. Kwa does not specify the circuit components to be a processor and a SLDRAM memory and does not provide details as to how the circuitry is powered.

29. Kimmel teaches:

- Having insertable cards with supporting a processor and a memory (Column 2, Lines 19-22).
- Supporting a power supply in the housing (Column 1, Lines 17-19).
- Coupling the power supply to the processor via the first slot connector (Figure 3, Item 106), the coupling including using circuit traces on the first card extending from the edge connector of the first card toward the processor (Figure 3, Item 64).

- Coupling the power supply to the memory via the second slot connector (Figure 3, Item 106), the coupling including using circuit traces on the second card extending from the edge connector of the second card toward the memory (Figure 3, Item 64),

30. Kimmel is motivated to allow for the removal of a single card in a system containing a plurality of such cards without affecting the remainder of the system (Column 1, Lines 34-38).

31. Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate the teaching of Kimmel into the system disclosed by Kwa and Swirhun for the benefit of allowing single cards in the multiple card system to be removed without affecting the performance of the remainder of the system.

32. Kimmel does not specify the memory device to be a SLDRAM memory device.

33. Gillingham teaches synchronous link DRAM (Pages 29-39) meets the high data bandwidth requirements of emerging processor architectures and retains the low cost of earlier DRAM interface standards (Page 29, Column 1, Paragraph 2).

34. Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of invention to further combine the teachings of SLDRAM as presented by Gillingham into the system so as to make use of memory that can support emerging processor architecture while still maintaining a low degree of cost.

35. Regarding Claims 15, 20, 32 and 36, Kimmel further teaches a third card in a third one of the connectors (Figure 1, Item 18), a co-processor supported by the third card (Column 2, Lines 19-22). Kimmel does not teach coupling the co-processor and processor with an optical interconnect.

36. Kwa further discloses an optical interconnect coupling a first circuit component to the second circuit component (Figure 1, Item 130; Column 1, Lines 11-22).

37. Regarding Claims 16, 21, 33 and 37, Kimmel further teaches conductors coupling the power supply to the co-processor via the third connector (Figure 3, Item 106), the conductors including circuit traces on the third card (Figure 3, Item 64).

38. Regarding Claims 18 and 23, Kwa further discloses including an electronic device in the housing capable of generating electromagnetic interference (Figure 1, Item 142), and wherein the optical interconnect shields communications between the processor and the memory from the electromagnetic interference (Figure 1, Item 142; the electric connections are capable of generating interference, which, by virtue of the optical connection being disposed apart from these electrical connections, are substantially inhibited from interfering with the memory/process intercommunications).

39. Claims 17, 22, 34 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimmel, Gillingham and Kwa as applied to claims 15, 20, 32 and 36 above, and further in view of Freedman (4839829).

40. Kimmel, Gillingham and Kwa taught each and every limitation as discussed above in reference to claims 15, 20, 32 and 36. Kimmel, Gillingham and Kwa did not disclose explicitly a math co-processor.

41. Freedman teaches a math co-processor (Column 5, Lines 66-68) to enhance floating point computational speeds (Column 5, Lines 66-68).

42. Accordingly, it would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate a math co-processor as taught by Freedman into the system

taught by Kimmel, Gillingham and Kwa for the benefit of enhance floating point computational speeds.

Response to Arguments

43. Applicant's arguments with respect to claims 1 and 24 have been considered but are moot in view of the new ground(s) of rejection as necessitated by amendment.

44. Applicant's arguments with respect to other claims have been fully considered but they are not persuasive as demonstrated below.

45. Applicant alleges that "it would not be obvious to substitute a portion of the structure of ... for portions of the structure of ... because there is no teaching in the reference themselves of how the components should be combined..." Examiner disagrees and submits that the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ***ordinary skill in the art***. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In the instant case, Examiner submits that the combined references teach each and every limitation of the claims as discussed above and that one with ordinary skill in the art would have combined the structures appropriately for proper functioning.

46. Applicant alleges that "there are no teachings in the references themselves which teach that there would be any advantage resulting from selecting portions of the structure of ... and integrating that structure somehow into the structure of ...". Examiner disagrees and submits that explicit motivations were provided as discussed above [Kimmel advocates the advantage of the removal of a single card in a system containing a plurality of such cards without affecting the

remainder of the system via the use of memory components; Gillingham teaches synchronous link DRAM meets the high data bandwidth requirements of emerging processor architectures and retains the low cost of earlier DRAM interface standards.

47. Applicant alleges that "even if the references could be combined... no teaching or suggestion ... as to what sort of signals should be sent optically instead of through circuit traces". Examiner disagrees and submits that the features upon which applicant relies (i.e., specific signals sent optically or through circuit trances) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

48. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
November 2, 2005

LYNNE H. BROWNE
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